AMENDMENT TO THE CLAIMS

1. (Currently Amended) A semiconductor memory device having semiconductor memory chips, each semiconductor memory chip comprising:

a plurality of memory banks capable of independently ~~to be~~ being accessed, each memory bank having a plurality of memory blocks, wherein at least two of the memory blocks, which are adjacent to each other in the same memory bank, have ~~the~~ different numbers of unit memory blocks, so that each memory bank has a non-rectangular shape.

2. (Original) The semiconductor memory device as recited in claim 1, further comprising a plurality of pads and control blocks arranged in a vacant space between neighboring memory banks.

3. (Currently Amended) The semiconductor memory device as recited in claim 1, wherein each of the memory blocks includes a pair of X-decoder and Y-decoder.

4. (Currently Amended) The semiconductor memory device as recited in claim 1, wherein each memory bank includes an odd ~~numbers~~ number of the memory blocks.

5. (Currently Amended) The semiconductor memory device as recited in claim 1, wherein a total memory region of the semiconductor memory chip is divided into four memory banks, wherein the four memory banks are arranged ~~to~~ in the first, second, third and fourth quadrants of the semiconductor memory chip, respectively.

6. (Currently Amended) The semiconductor memory device as recited in claim 5, wherein each memory bank includes:

a first memory block having a first ~~numbers~~ number of the unit memory blocks;

a second memory block having a second ~~numbers~~ number of the unit memory blocks, which is smaller than that of the first memory blocks; and

a third memory block having the second ~~numbers~~ number of the unit memory blocks.

7. (Original) The semiconductor memory device as recited in claim 6, wherein the first memory blocks of memory banks arranged in the second and third quadrants are arranged at a left-most region of the semiconductor memory chip and the first memory block of banks arranged in the first and fourth quadrants is arranged at a right-most region of the semiconductor memory chip.

8. (Original) The semiconductor memory device as recited in claim 7, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

9. (Original) The semiconductor memory device as recited in claim 6, wherein each first memory block of each memory bank is arranged by being neighbored in a central region of the semiconductor memory chip.

10. (Original) The semiconductor memory device as recited in claim 9, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

11. (Original) The semiconductor memory device as recited in claim 6, wherein each first memory block of each memory bank is arranged in a central region of each bank, respectively.

12. (Original) The semiconductor memory device as recited in claim 11, further comprising a plurality of pads and control blocks arranged between the neighboring

second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

13. (Currently Amended) The semiconductor memory device as recited in claim 6, wherein each of the first, second and third memory blocks has a pair of X-decoder and Y-decoder, respectively, and a final driving terminal of the X-decoder in the first memory ~~blocks~~ block is separated into two driving terminals.

14. (Currently Amended) The semiconductor memory device as recited in claim 6, wherein the first memory block includes six 8-Mbit unit memory blocks, and each of the second and the third memory blocks includes five 8-Mbit unit memory blocks.

15. (Currently Amended) The semiconductor memory device as recited in claim 5, wherein each memory bank includes:

a first memory block having a first ~~numbers~~ number of the unit memory blocks;

a second memory block having a second ~~numbers~~ number of the unit memory blocks, which is smaller than that of the first memory block; and

a third memory block having the first ~~numbers~~ number of the unit memory blocks.

16. (Original) The semiconductor memory device as recited in claim 15, wherein the second memory blocks of memory banks arranged in the second and third quadrants are arranged at a left-most region of the semiconductor memory chip and the second memory blocks of banks arranged in the first and fourth quadrants are arranged at a right-most region of the semiconductor memory chip.

17. (Original) The semiconductor memory device as recited in claim 16, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

18. (Original) The semiconductor memory device as recited in claim 15, wherein each second memory block of each memory bank is arranged by being neighbored in a central region of the semiconductor memory chip.

19. (Original) The semiconductor memory device as recited in claim 18, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

20. (Original) The semiconductor memory device as recited in claim 15, wherein each second memory block of each memory bank is arranged in a central region of each bank, respectively.

21. (Original) The semiconductor memory device as recited in claim 20, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

22. (Original) The semiconductor memory device as recited in claim 15, wherein each of the first, second and third memory blocks has a pair of X-decoder and Y-decoder, respectively, and a final driving terminal of the X-decoder in the first and the third memory blocks is separated into two driving terminals.

23. (Original) The semiconductor memory device as recited in claim 15, wherein each of the first and the third memory blocks includes six 8-Mbit unit memory blocks and the second memory blocks includes five 8-Mbit unit memory blocks.

24. (Currently Amended) A semiconductor memory device having a semiconductor memory chip divided into 18 regions having an equal area in a 3 rows X 6 columns array, the semiconductor memory chip comprising:

a first memory bank including memory blocks arranged at one region selected from a first group including a 2nd row X 1st column region, a 2nd row X 2nd column region and a 2nd row X 3rd column region and at a 1st row X 1st column region, a 1st row X 2nd column region and a 1st row X 3rd column region;

a second memory bank including memory blocks arranged at one region selected from the first group except for the region included in the first memory bank ~~a 2nd row X 1st column region, a 2nd row X 2nd column region and a 2nd row X 3rd column region~~ and at a 3rd row X 1st column region, a 3rd row X 2nd column region and a 3rd row X 3rd column region;

a third memory bank including memory blocks arranged at one region selected from a second group including a 2nd row X 4th column region, a 2nd row X 5th column region and a 2nd row X 6th column region and at a 1st row X 4th column region, a 1st row X 5th column region and a 1st row X 6th column region;

a fourth memory bank including memory blocks arranged at one region selected from the second group except for the region included in the third memory bank ~~a 2nd row X 4th column region, a 2nd row X 5th column region and a 2nd row X 6th column region~~ and at a 3rd row X 4th column region, a 3rd row X 5th column region and a 3rd row X 6th column region; and

pads and control blocks arranged at one region selected from the first group except for the regions included in the first and second memory bank and the second group except for the regions included in the third and fourth memory bank, ~~the 2nd row X 1st column region, the 2nd row X 2nd column region, the 2nd row X 3rd column region, the 2nd row X 4th column region, the 2nd row X 5th column region and the 2nd row X 6th column region~~

wherein said each memory bank has a non-rectangular shape.

25. (Currently Amended) The semiconductor device as recited in claim 24, wherein ~~a~~ an X-decoder between the neighboring memory blocks in the same memory bank is shared each other.

26. (Original) The semiconductor device as recited in claim 24, wherein the pads are arranged between the first and second banks and the third and fourth banks.

27. (Currently Amended) A method for arranging memory blocks to a semiconductor memory chip in a semiconductor device, comprising of:

configuring a plurality of memory blocks with a plurality of neighboring unit memory blocks; and

configuring a plurality of memory banks with the neighboring memory blocks, wherein at least two of the memory blocks have different numbers of unit memory blocks ~~each other~~ in the same bank so that each memory bank has a non-rectangular shape.

28. (Currently Amended) The method as recited in claim 27, wherein pads and control blocks are arranged between the memory blocks relatively having a smaller number of unit memory blocks.